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Addressing Package Voids on Extremely Small Leadframe Device

A. Sumagpang Jr.[1*] and F. R. Gomez[1]

[1]New Product Development and Introduction, STMicroelectronics, Inc., Calamba City, Laguna, 4027, Philippines.

Authors' contributions

This work was carried out in collaboration between both authors. Both authors read, reviewed and approved the final manuscript.

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ABSTRACT

The paper focused in addressing the package voids defect of a semiconductor device utilizing an extremely small leadframe technology. Potential risk analysis and pareto diagram were completed to identify the top reject contributors and eventually come-up with the robust solution. A comprehensive design of experiments (DOE) was completed and solution validation was performed to formulate the effective corrective actions. Results revealed that package voids were addressed by optimizing the molding process focusing on the molding temperature and curing time. A significant improvement of 95 % for package voids reduction was achieved. For future works, the parameters and learnings could be used on devices with similar configuration.

Keywords: Compression molding; leadframe; line-stressing; package voids; semiconductor.

1. INTRODUCTION

New trends and continuous development in semiconductor technology offer great challenges in assembly manufacturing industry. An imperative challenge for any industry is to maintain its competitive market position and value. Important to note that failure to provide customer expectation in terms of quality and time-to-market would result to possible business failure. This critical situation should really be prevented that is why a line-stressing is being

**Corresponding author: Email: antonio.sumagpang@st.com;*

employed in preparation to mass or full-production mode.

The device in focus is a newly-introduced leadframe package in the plant having an extremely small footprint as illustrated in Fig. 1. The device functions as a diode with a single wire connection, for mobile phones and computer applications. Regardless of its simple geometry, it is considered as a critical device as state-of-the-art platforms are needed to meet its output process.

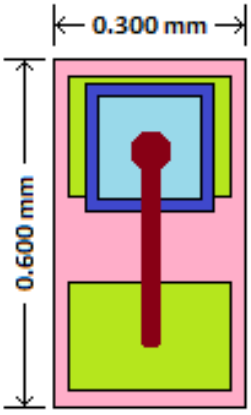


Fig. 1. Device dimension

The device has a very thin die and with extremely small total package dimension. The assembly manufacturing process includes a step-cutting method of wafers, compression molding, and in-strip testing, that are not commonly used in other semiconductor industries. A part of the assembly process flow is shown in Fig. 2. Worthy to note that assembly and test process flow varies with the product and the technology [1-4]. With the continuing technology development and state-of-the-art platforms, challenges in semiconductor industry are inevitable [5-8].

Assembly defects were encountered during the line-stressing and ramp-up of the device. Critical processes were identified using risk analysis, and one of which focused on the molding process as identified in Table 1. Evaluation was completed before the risk build to accelerate confidence on line-stressing. Moreover, potential risk analysis was given contingency plans and established corrective actions.

Reject contributors on the identified critical processes are shown in Fig. 3 chart. Molding is one critical process identified with output abnormalities as a result of unoptimized parameters which are typically attributed to newly-introduced devices.

Of the 21 % defect contribution of the molding process, pareto diagram in Fig. 4 shows package voids or mold voids as the top reject parts per million (ppm) contributor. Parameter optimization is one of the factors to be checked as the device has no other similar product in the plant for reference. Benchmarking from other semiconductor plants is being considered to have a reference or baseline for critical process parameters.

Top rejects based on pareto diagram substantially affect the yield and delivery during line-stressing performance. With this, process optimization is highly recommended at line-stressing before it reaches the full-production mode. Table 2 shares the top defect signature of the molding process. Further investigation and analysis of failures were done by collecting the actual reject samples at this critical process. This eventually is essential in developing the corrective actions and improvement.

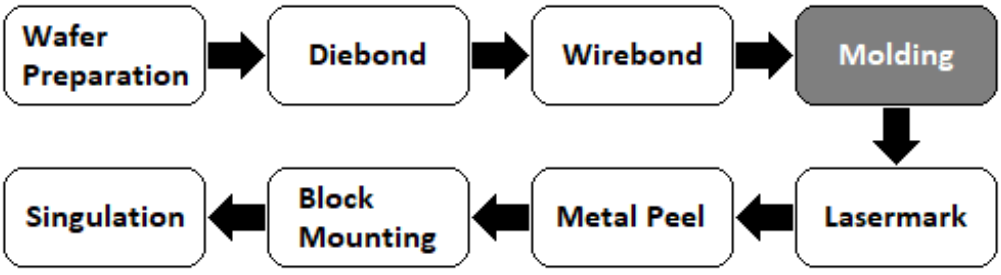


Fig. 2. Assembly process flow

Table 1. Potential risk analysis at molding process

Identified risk	Resulting potential risk	Evaluation before action			Identified action
		Probability	Impact	Class	
0.3 mm package molding, package molding defects, voids, incomplete fill	• Low yield • Reliability	9	9	A	Capability using compression molding technology

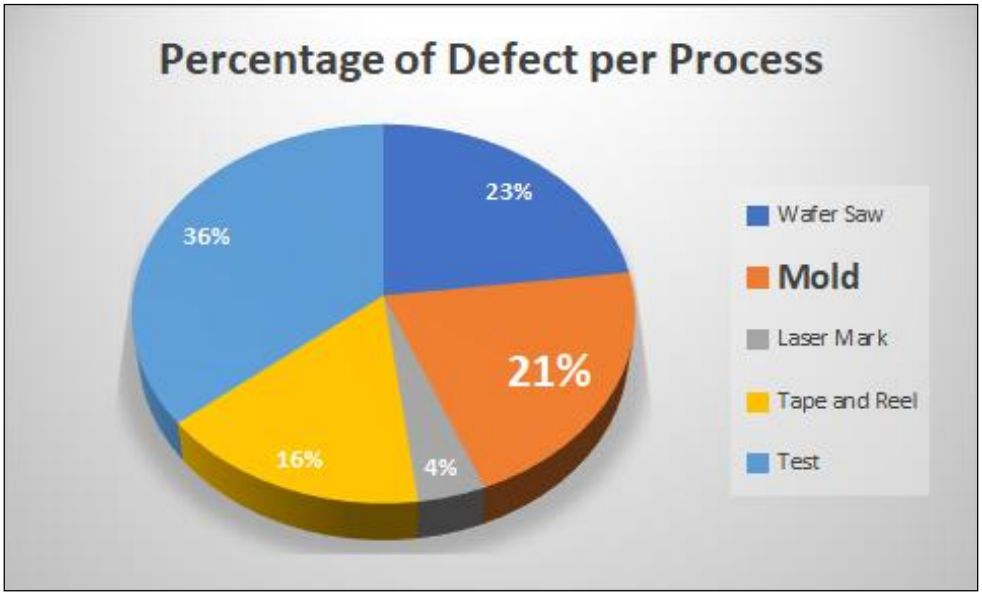


Fig. 3. Defect contribution per assembly process

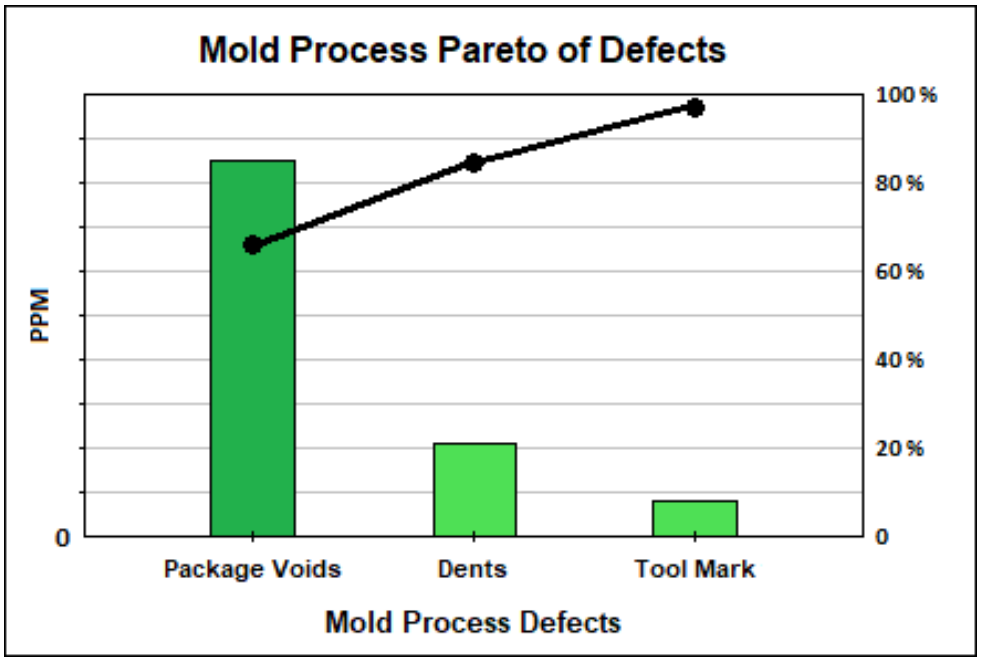


Fig. 4. Pareto diagram of mold process rejects with package voids as top contributor

2. LITERATURE REVIEW

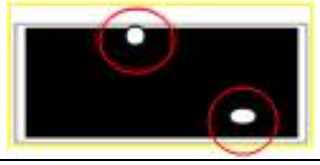
One of the fundamental components in the production of semiconductor devices is the molding compound, which is a packaging material for encapsulation to protect the device from external environment [9]. The device uses compression molding as illustrated in Fig. 5.

The advantages of compression molding system are zero to less wire damage, good filling on narrow gap on die, and no cull or runner. The technology was necessary for the device due to the constraint of narrow mold cap thickness. With this, the device is susceptible to voids during molding, thus package voids became the top reject contributor. Package voids are usually easy to address, but this would require a comprehensive parameter optimization through design of experiments (DOE). Ultimately, DOE was done to achieve the desired parameter range for molding process considering the critical input and output responses, with the package voids as the primary output response.

3. METHODOLOGY

DOE evaluation for compression molding was conducted with the intent to determine and define window for critical parameter range that would eliminate package voids. Shown in Table 3 is the DOE evaluation matrix prepared using a statistical software that automatically provides the combination of runs.

Table 2. Top defect signature of molding process

Critical process	Top defect signature	Criteria	Remarks
Molding process	Package voids 	Not allowed	Failed

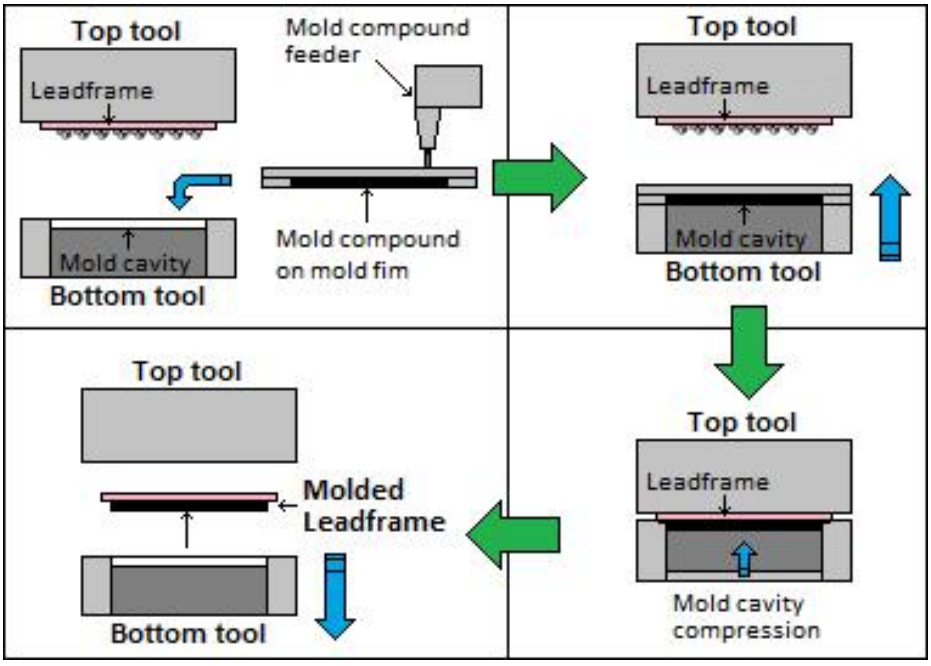


Fig. 5. Compression molding mechanism

Table 3. DOE evaluation matrix

Run	Pattern	Mold temperature (°C)	Cure time (s)	Package voids
1	1-1	170	160	Output response to be measured
2	1-2	170	180	
3	1-3	170	200	
4	2-1	175	160	
5	2-2	175	180	
6	2-3	175	200	
7	3-1	180	160	
8	3-2	180	180	
9	3-3	180	200	

Full-factorial design with a total of nine runs was created. Using the statistical software tool, mold temperature and cure time were identified as the most critical parameters that affect package voids occurrence. Results are discussed in the succeeding section.

4. RESULTS AND ANALYSIS

During development, the initial problem encountered was package voids in every shot. Together with the mold machine field support and the mold compound technical support, DOE was performed using a matrix of different batches of mold compound and sets of mold parameters, as shared in Fig. 6.

DOE results of compression molding showed that optimum parameters in terms of package voids can be achieved by using the 175°C and 180 seconds curing time regardless of molding compound used.

After the implementation of the identified solutions and corrective actions, level of rejections was monitored. Fig. 7 depicts the improvement in the ppm level. Actual ppm values are intentionally not shown due to confidentiality.

An improvement of 95 % for die chippings reduction was achieved through the comprehensive DOE. Assembly yield trend stabilized after the implementation, optimization, and sustainability of the improvement and all corrective actions. Importantly, this indicates manufacturing preparedness for full-production mode.

Molding Type			Transfer Mold	Compression Mold			
Mold Compound			TM1	CM1	CM2	CM3	CM4
Powder sieving		-	No	150um on 1mm pass			
Spiral flow		inch	33	55	55	50	53
Flash length		mm	1.1	1.7	1.7	1.7	1.4
Hot hardness(90sec)		-	88	72	72	83	86
Gelation time(175C)		sec	32	75	90	102	93
Viscosity(175C)		poise	230	140	140	260	270
Disk flow		mm	78	94	94	91	91
Tg		degC	135	135	135	130	125
CTE	alpha-1	ppm/C	8	7	7	8	7
	alpha-2	ppm/C	30	27	27	30	27
Flexural Modulus		kgf/mm2	2400	2400	2400	2600	2600
Flexural Strength		kgf/mm2	15	14	15	15	15
Water absorption		%	0.23	0.23	0.23	0.27	0.28
Mold shrinkage		%	0.06	0.06	0.06	0.05	0.11

Need longer cure time such as 175℃/180s

Fig. 6. DOE matrix for compression molding process optimization

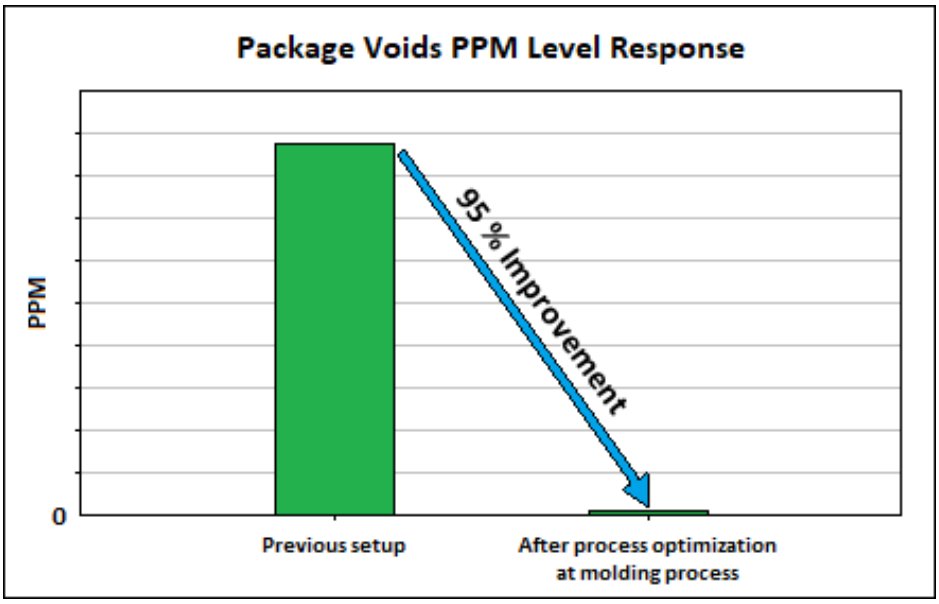


Fig. 7. Improvement after optimization and implementation of corrective actions

5. CONCLUSION AND RECOMMENDATIONS

Comprehensive engineering analyses with the aid of statistical analysis were done in solving and addressing the package voids of an extremely small device at molding process. Through DOE, parameters optimization was formulated, with package voids occurrence significantly minimized by achieving the optimum molding temperature and curing time. A 95 % improvement for package voids reduction was ultimately achieved.

Process optimization plays an essential role to as early as line-stressing stage, before full-production release can be granted. It is imperative that when newly-introduced devices are coming in, critical processes should be identified and that appropriate improvement, corrective actions, and solutions be made so that when full-production is set, both quality and speed could be achieved. Techniques and learnings shared in this paper could be used for future works on semiconductor devices with comparable configuration. Also, studies and works discussed in [10-12] are helpful in improving the assembly processes particularly in the yield improvement.

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COMPETING INTERESTS

Authors have declared that no competing interests exist.

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